



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/050,347
Filing Date January 15, 2002
Inventor Gurtej S. Sandhu et al.
Assignee Micron Technology, Inc.
Group Art Unit 2813
Examiner Schillinger, L.
Attorney's Docket No. MI22-1897
Title: Methods of Forming Transistors

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge

07/13/2004 AJOHNS01 00000012-230925 10050347
01 FC:1806 the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit 180.00 DA

Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

Date: June 4, 2003

RECEIVED
JUN 10 2003
CHNOLOGY CENTER 2800